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To:	Kevin Burd	From:	Asian Ettehadieh	
Fax:	571-273-3008	Date:	November 7, 2008	
Phone:		Pages:	7 (including cover sheet)	
Your Ref.:	10/761,272	Our Ref.:	0951-0131P	
Re:	Interview	CC:		

Urgent For Review Please Comment Please Reply Please Recycle

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Comments:

Applicant Initiated Interview Request Form

Application No.: 10/761272	First Named Applicant: Fukae, Fumihiro
Examiner: Burd, Kevin M.	Art Unit: 2611 Status of Application: pending

Tentative Participants:

(1) Kevin Burd	(2) Aslan Ettehadieh
(3)	(4)

Proposed Date of Interview: Wednesday, November 12, 2008 Proposed Time: 10:00 a.m.

Type of Interview Requested:

(1) Telephonic (2) Personal (3) Video Conference

Exhibit To Be Shown or Demonstrated: [] YES [] NO
If yes, provide brief description:

Issues To Be Discussed

Issues (Rej., Obj., etc)	Claims/ Fig. #s	Prior Art	Discussed	Agreed	Not Agreed
(1) 103 Rej.	Indep. claims	Chawla	[]	[]	[]
(2)			[]	[]	[]
(3)			[]	[]	[]
(4)			[]	[]	[]

[x] Continuation Sheet Attached

Brief Description of Arguments to be Presented:

Primary Examiner Burd: please see attached sheet.

An interview was conducted on the above-identified application on

**NOTE: This form should be completed by applicant and submitted to the examiner in advance of the interview
(see MPEP § 713.01).**

This application will not be delayed from issue because of applicant's failure to submit a written record of this interview. Therefore, applicant is advised to file a statement of the substance of this interview (37 CFR 1.133(b)) as soon as possible.

Applicant/Applicant's Representative Signature

Examiner/SPE Signature

Typed/Printed Name of Applicant or Representative

62,278

Registration Number, if applicable

This collection of information is required by 37 CFR 1.133. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 21 minutes to complete, the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450

CURRENT CLAIM 1 – EMPHASIS ADDED

1. (Previously presented) A transceiver circuit capable of transferring data at one or more transfer rates, the transceiver circuit comprising:

one or more state machines having one or more tone phases in which determination of a maximum transfer rate for one or more channels and one or more connections with one or more remote devices is carried out through exchange of one or more tone signals with at least one of the remote device or devices, and one or more data transfer phases in which data transfer is carried out at one or more frequencies higher than that of at least one of the tone signal or signals;

one or more error detection circuits detecting one or more errors in one or more receive signals; and

one or more data transfer phase transition suppressor circuits;

wherein, in the event that at least one of the error detection circuit or circuits detects at least one of the error or errors within at least one of the receive signal or signals during at least one of the data transfer phase or phases, one or more transitions is made from at least one of the data transfer phase or phases to at least one of the tone phase or phases, and after at least one of such transition or transitions has occurred, at least one of the data transfer phase transition suppressor circuit or circuits carries out control so as to prevent transition back to at least one of the data transfer phase or phases.

PROPOSED AMENDMENTS TO THE CLAIMS

1. (Currently amended) A transceiver circuit capable of transferring data at one or more transfer rates, the transceiver circuit comprising:

one or more state machines having one or more tone phases in which determination of a maximum transfer rate for one or more channels and one or more connections with one or more remote devices is carried out through exchange of one or more tone signals with at least one of the remote device or devices, and one or more data transfer phases in which data transfer is carried out at one or more frequencies higher than that of at least one of the tone signal or signals;

Application No. 10/761,272

Docket No.: 0951-0131P

one or more error detection circuits detecting one or more errors in one or more receive signals; and

one or more data transfer phase transition suppressor circuits;

wherein, in the event that at least one of the error detection circuit or circuits detects at least one of the error or errors within at least one of the receive signal or signals during at least one of the data transfer phase or phases, one or more transitions is made from at least one of the data transfer phase or phases to at least one of the tone phase or phases, and after at least one of such transition or transitions has occurred, at least one of the data transfer phase transition suppressor circuit or circuits carries out control so as to prevent transition back to at least one of the data transfer phase or phases while either remaining in the tone phase or proceeding to at least one of a speed negotiation phase or phases.

4. (Currently amended) A transceiver circuit capable of transferring data at one or more transfer rates, the transceiver circuit comprising:

one or more state machines having one or more tone phases in which one or more connections with one or more remote devices are established through exchange of one or more tone signals with at least one of the remote device or devices, one or more speed negotiation phases in which determination of the maximum transfer rate permitted by one or more channels is carried out through mutual notification of one or more transfer rates of which the local device is capable, this notification being actually carried out at at least one of such transfer rate or rates, and one or more data transfer phases in which data transfer is carried out at at least one of the transfer rate or rates determined at at least one of the speed negotiation phase or phases;

one or more error detection circuits detecting one or more errors in one or more receive signals; and

one or more speed negotiation phase transition suppressor circuits;

wherein, in the event that at least one of the error detection circuit or circuits detects at least one of the error or errors within at least one of the receive signal or signals during at least one of the data transfer phase or phases, one or more transitions is made from at least one of the data transfer phase or phases to at least one of the tone phase or phases and remaining in at least

Application No. 10/761,272

Docket No.: 0951-0131P

| one of the tone phase or phases until an error parameter is less than a value, and after at least one of such transition or transitions has occurred, at least one of the speed negotiation phase transition suppressor circuit or circuits carries out control so as to prevent transition to at least one of the speed negotiation phase or phases.

5. (Currently amended) A transceiver circuit capable of transferring data at one or more transfer rates, the transceiver circuit comprising:

one or more state machines having one or more tone phases in which one or more connections with one or more remote devices are established through exchange of one or more tone signals with at least one of the remote device or devices, one or more speed negotiation phases in which determination of one or more maximum transfer rates permitted by one or more channels is carried out through mutual notification of one or more transfer rates of which the local device is capable, this notification being actually carried out at at least one of such transfer rate or rates, and one or more data transfer phases in which data transfer is carried out at at least one of the transfer rate or rates determined at at least one of the speed negotiation phase or phases;

one or more error detection circuits detecting one or more errors in one or more receive signals; and

one or more speed negotiation phase transition suppressor circuits;

wherein, in the event that at least one of the error detection circuit or circuits detects at least one of the error or errors within at least one of the receive signal or signals during at least one of the speed negotiation phase or phases, one or more transitions is made from at least one of the data transfer phase or phases to at least one of the tone phase or phases and remaining in at least one of the tone phase or phases until an error parameter is less than a value, and after at least one of such transition or transitions has occurred, at least one of the speed negotiation phase transition suppressor circuit or circuits carries out control so as to prevent transition to at least one of the speed negotiation phase or phases.

Application No. 10/761,272

Docket No.: 0951-0131P

33. (Currently amended) A transceiver circuit capable of transferring data at a plurality of transfer rates, the transceiver circuit comprising:

one or more state machines having one or more tone phases in which one or more connections with one or more remote devices are established through exchange of one or more tone signals with at least one of the remote device or devices, one or more speed negotiation phases in which determination of the maximum transfer rate permitted by one or more channels is carried out through mutual notification of one or more transfer rates of which one or more local devices is capable, this notification being actually carried out at at least one of such transfer rate or rates, and one or more data transfer phases in which data transfer is carried out at at least one of the transfer rate or rates determined at at least one of the speed negotiation phase or phases;

one or more error detection circuits detecting one or more errors in one or more receive signals; and

one or more transfer rate comparison circuits comparing the minimum transfer rate of the transceiver circuit and one or more transfer rates employed during at least one of the data transfer phase or phases;

wherein, in the event that at least one of the error detection circuit or circuits detects at least one of the error or errors within at least one of the receive signal or signals during at least one of the data transfer phase or phases when at least one result of at least one comparison made by at least one of the transfer rate comparison circuit or circuits is that at least one of the transfer rate or rates employed during at least one of the data transfer phase or phases is greater than the minimum transfer rate or rates of the transceiver circuit, one or more transitions is made from at least one of the data transfer phase or phases to at least one of the tone phase or phases and remaining in at least one of the tone phase or phases until an error parameter is less than a value, and thereafter, the maximum transfer rate of the transceiver circuit during at least one of the speed negotiation phase or phases is set so as to be at least one rate that is lower than at least one transfer rate employed during at least one of the data transfer phase or phases.

Application No. 10/761,272

Docket No.: 0951-0131P

38. (Currently amended) A transceiving method, comprising:

determining a maximum transfer rate for at least one channel and at least one connection with at least one remote device through exchange of at least one tone signal with the at least one remote device;

transferring data at a frequency higher than that of the at least one of the tone signal; and detecting at least one error in at least one received signal;

wherein, in the event that an error is detected within the at least one received signal during at least one data transfer phase, at least one transition is made from the at least one data transfer phase to at least one tone phase, and after the at least one transition, control is carried out so as to prevent transition back to the at least one data transfer phase while either remaining in the tone phase or proceeding to at least one of a speed negotiation phase or phases.